Elektronika pre ATLAS experiment

Predstavenie

* Ing. Jaroslav Bán, CSc. vedecký pracovník ÚEF SAV Košice a senior stuff associate na Columbia University, New York, USA pracujúci na vývoji elektroniky pre experimenty vo fyzike vysokých energií.

Vyvinul som elektroniku, ktorá pracovala v experimentoch s ťažkými iónmi v Cerne, H1 experimente v Desy Hamburg, DO experimente vo Fermilabe a stále výborne pracuje v Atlas experimente v Cerne.

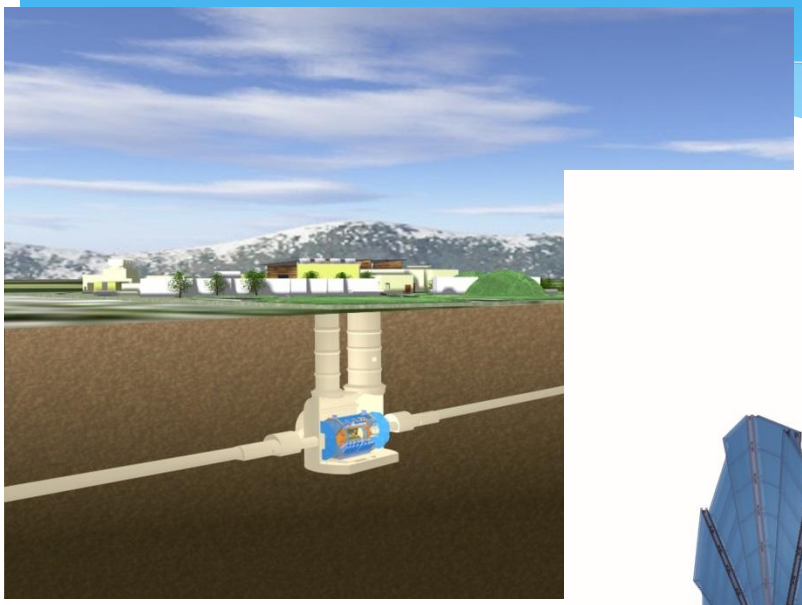
Vyvíjam radiačne odolné AD prevodníky pre Atlas trigger a Phase II upgrade.

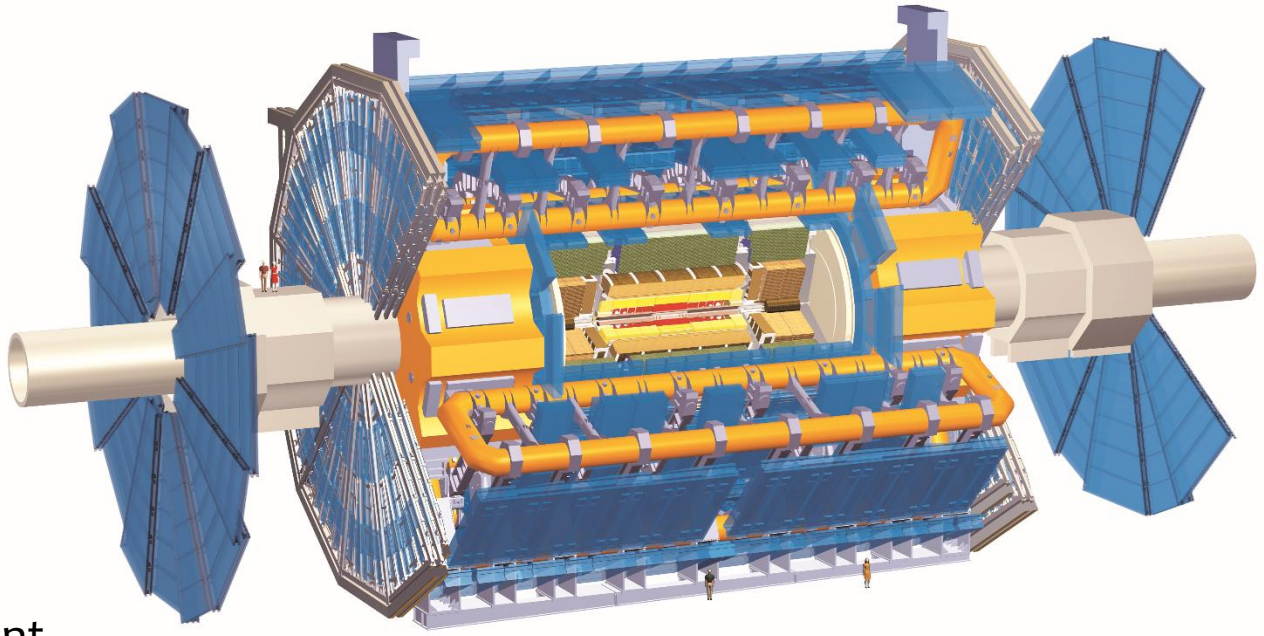
Úvod

Prednáška bude diskutovať iba radiačne odolnú elektroniku vyvinutú pre Atlas experiment:

* „Studená elektronika“ pre hadrónový end-cap Atlas-u
* Front-end elektronika pre Larg kalorimeter Atlas-u
* Radiačne odolný AD prevodník pre trigger a upgrade Atlas-u

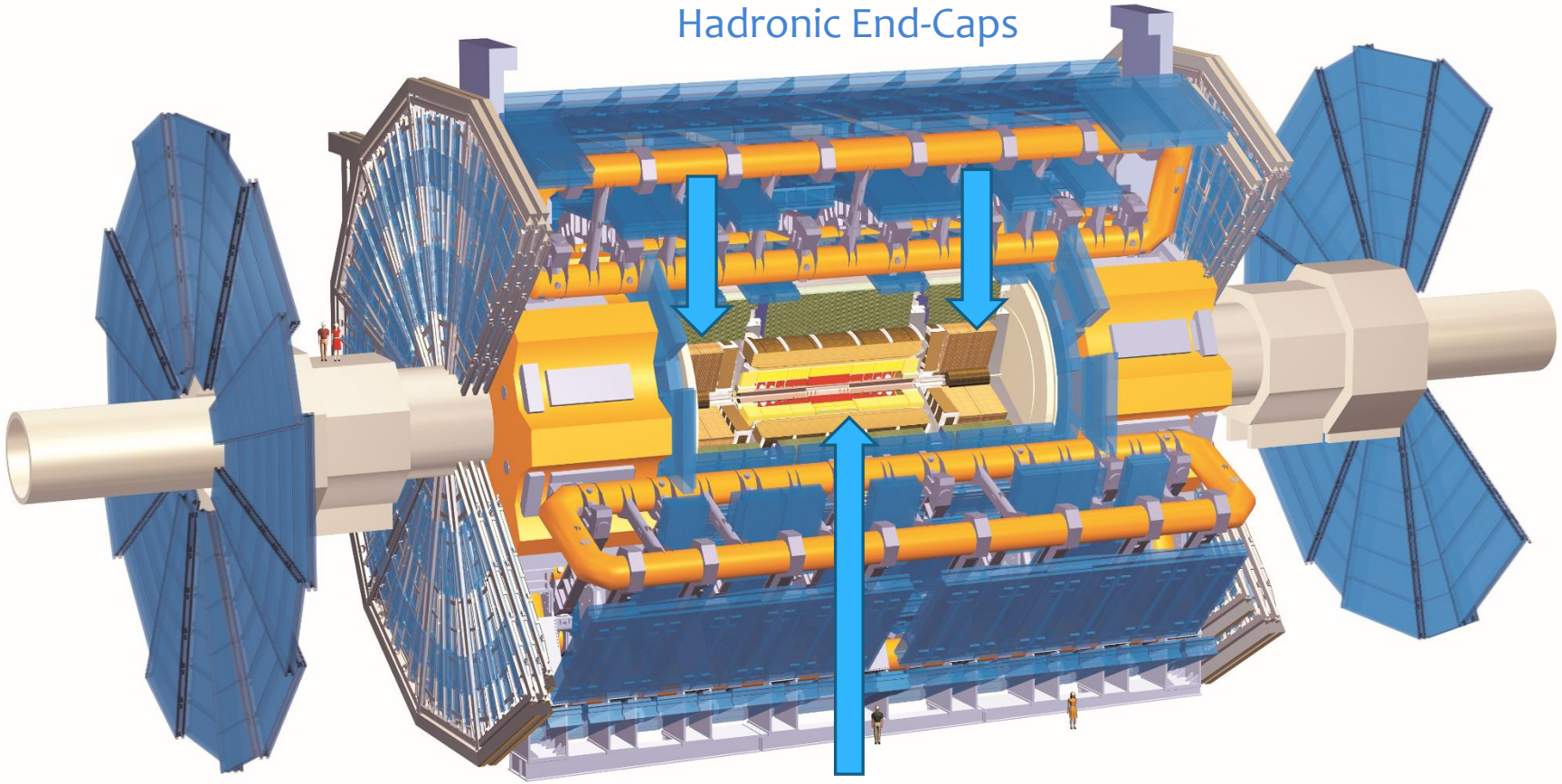
„Studená elektronika“ pre hadrónový end-cap Atlas-u

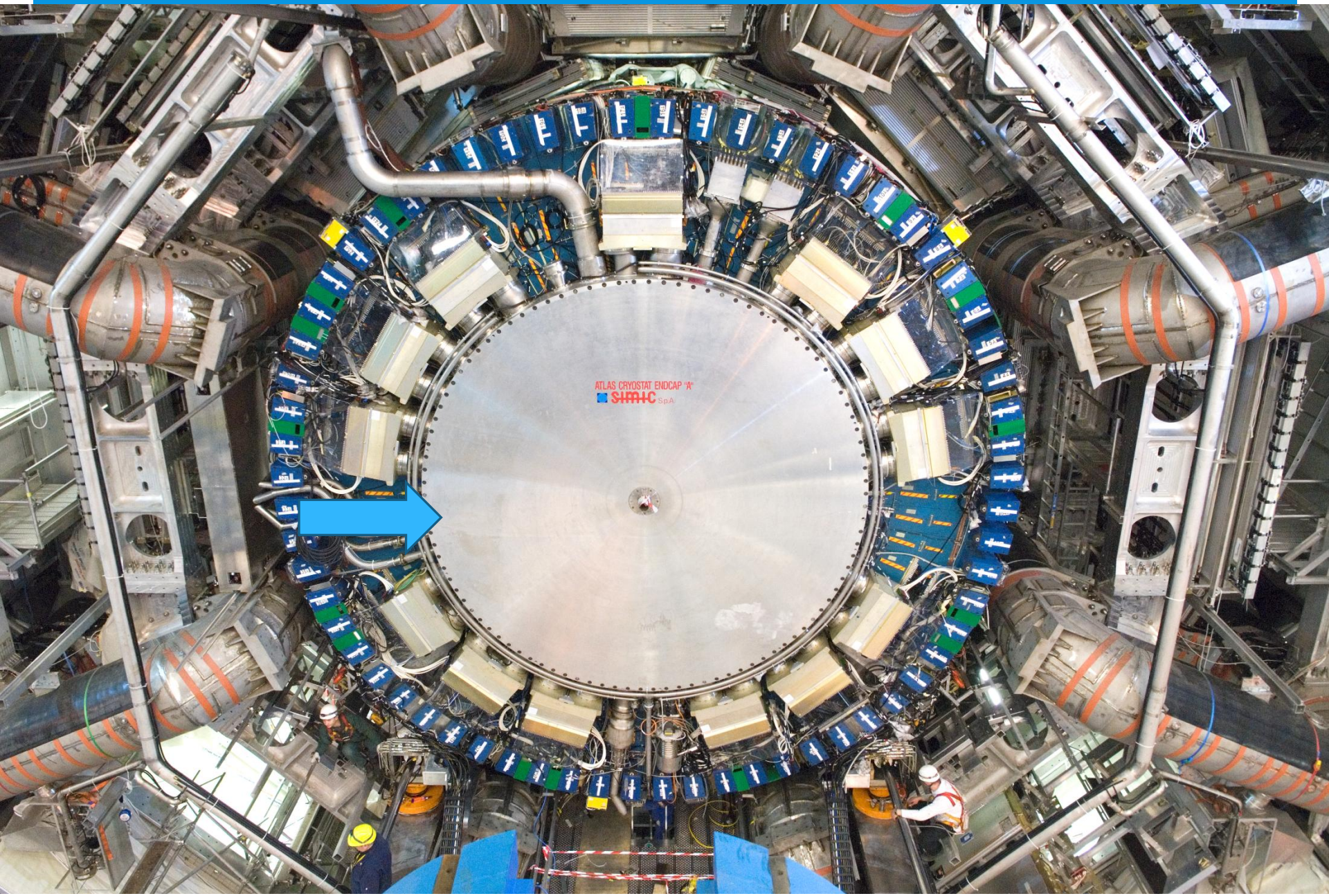




Atlas experiment

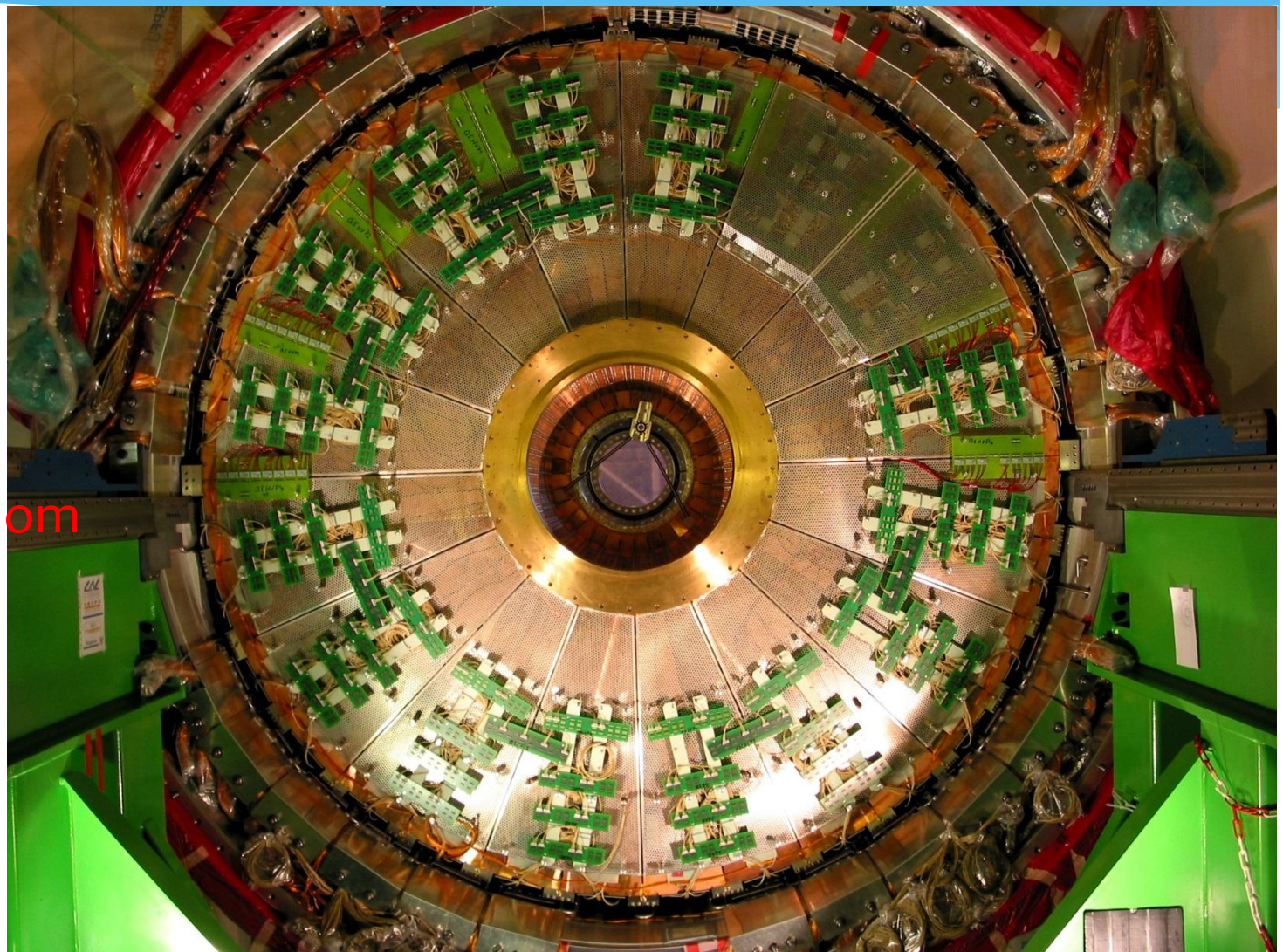
Atlas experiment



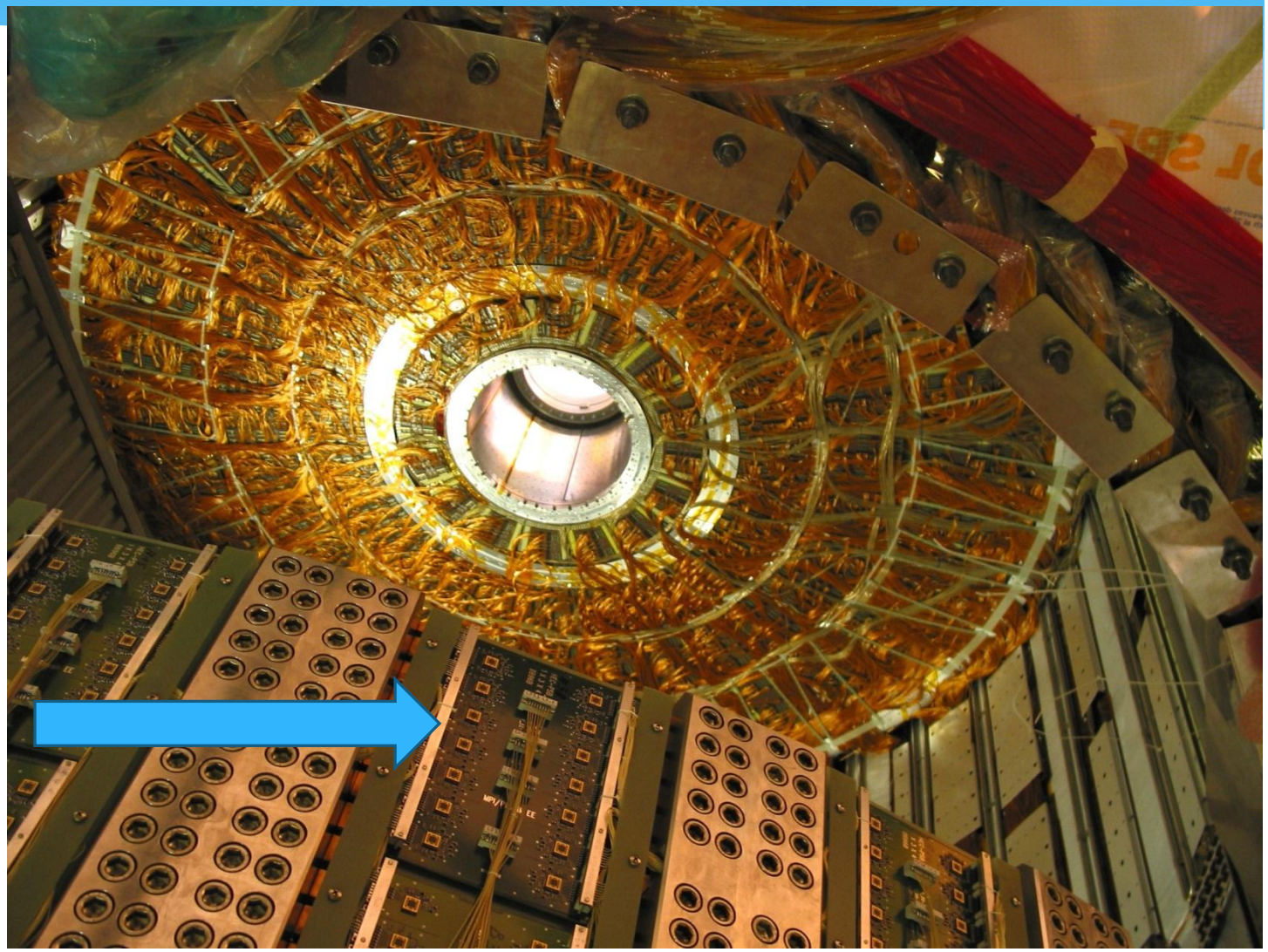

ATLAS CRYOSTAT ENDCAP "A"
SIMIC S.p.A.

Vnútro end-capu

Za normálnych podmienok napnené tekutým argónom (-200C).



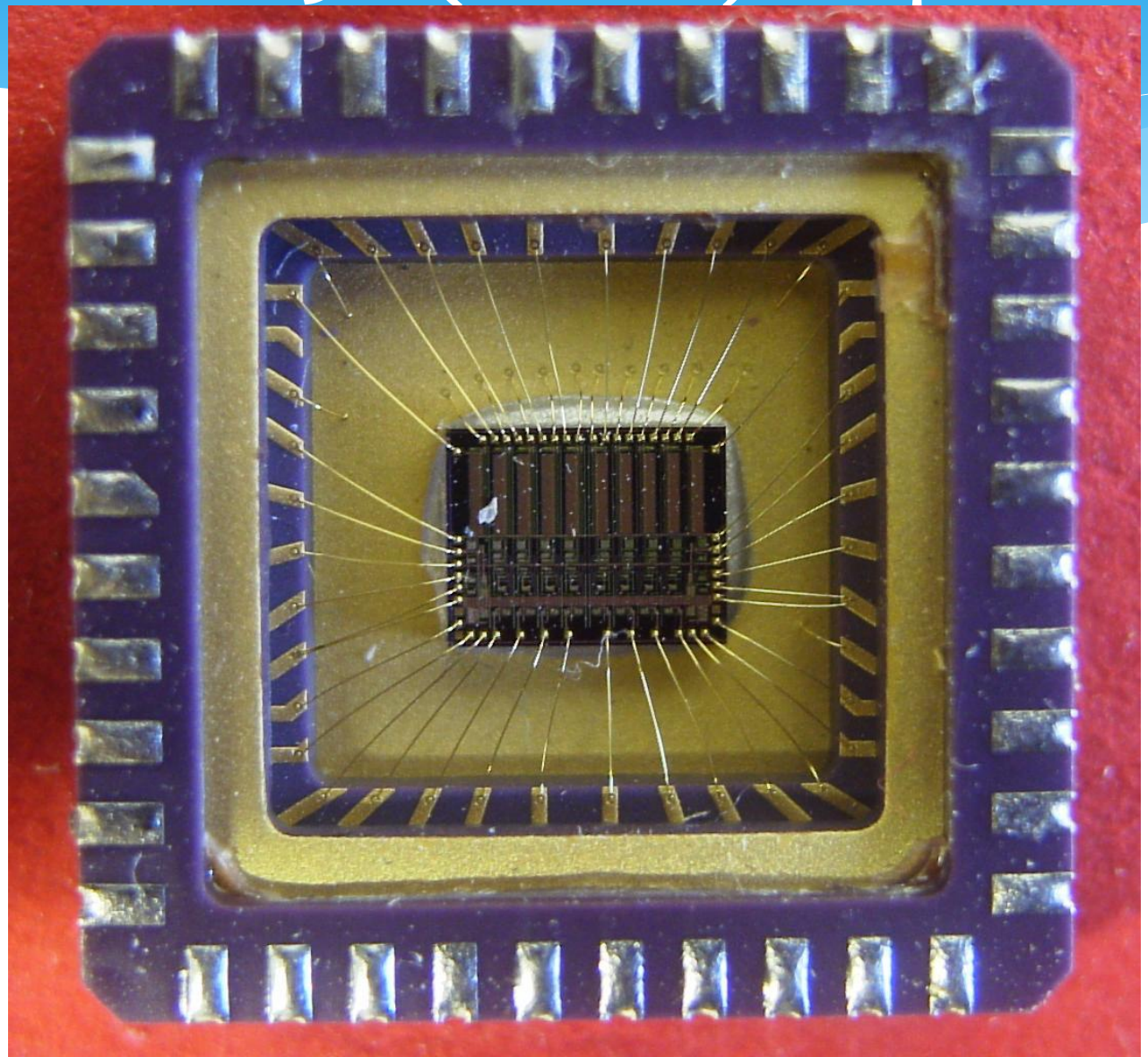
“Studená” elektronika vnútri end-capu



Dosky „studenej elektroniky“

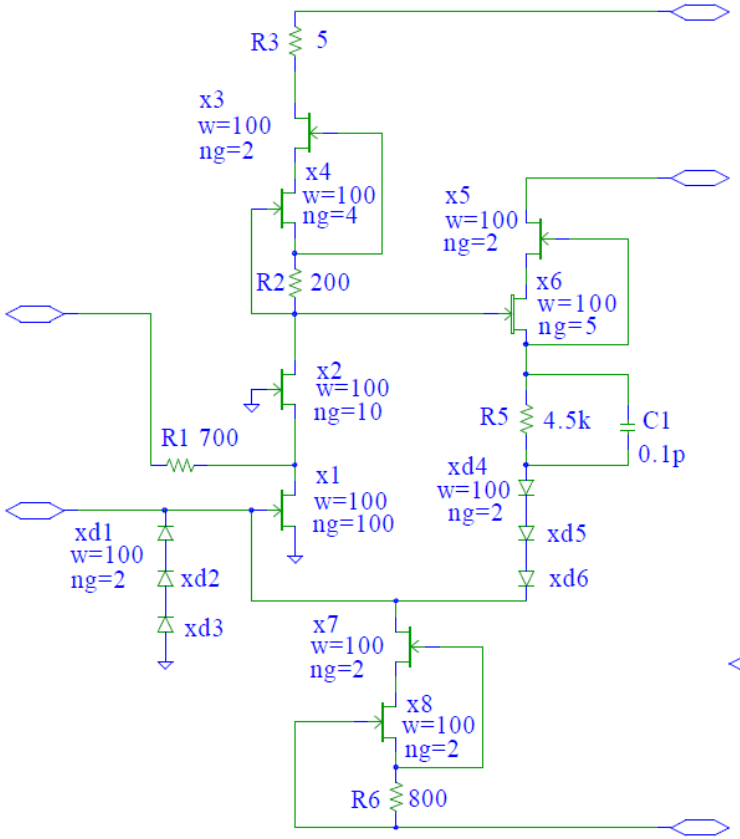
Púzdro BB96 (Ga-As) chipu

Základný stavebný prvok (12x12mm)

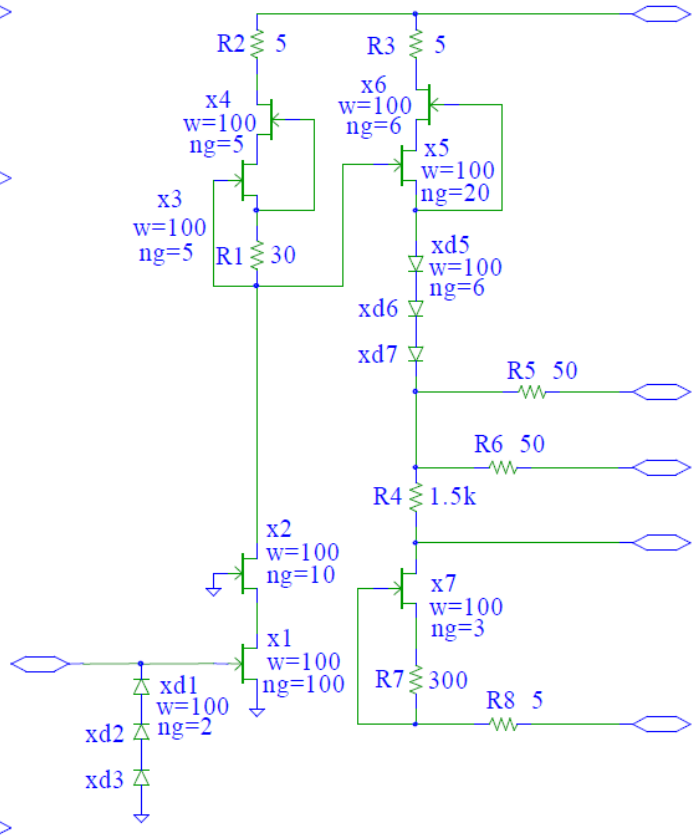


BB-96 chip schematics

1 um GaAs technológia

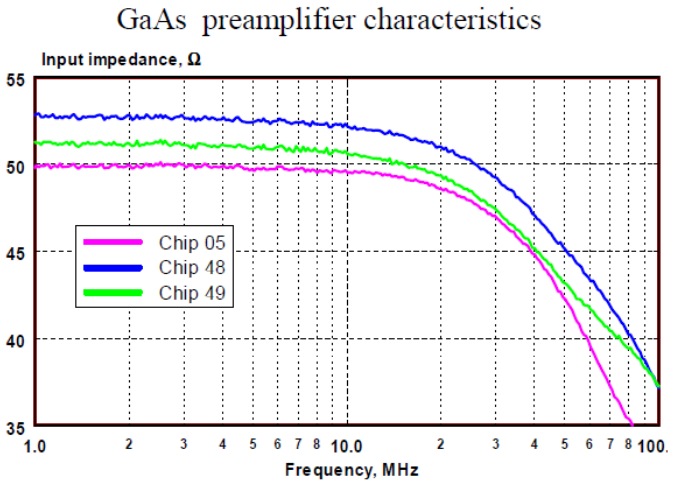


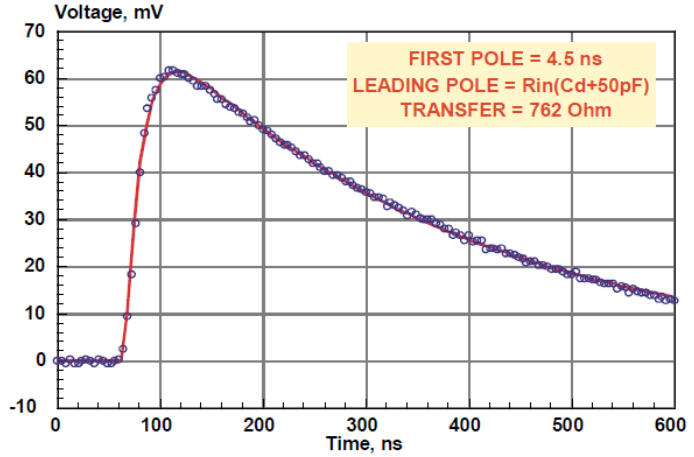
Predzosilňovač

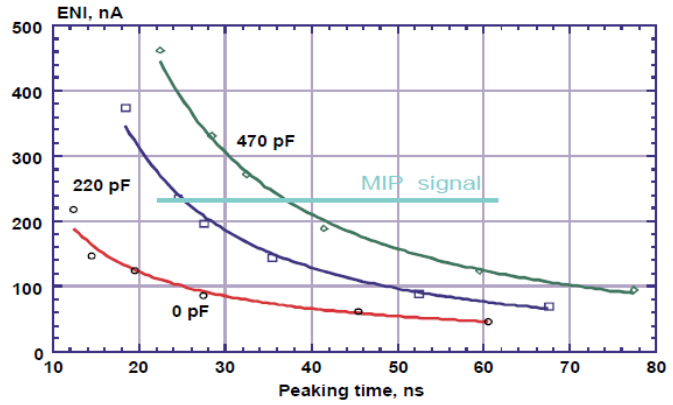


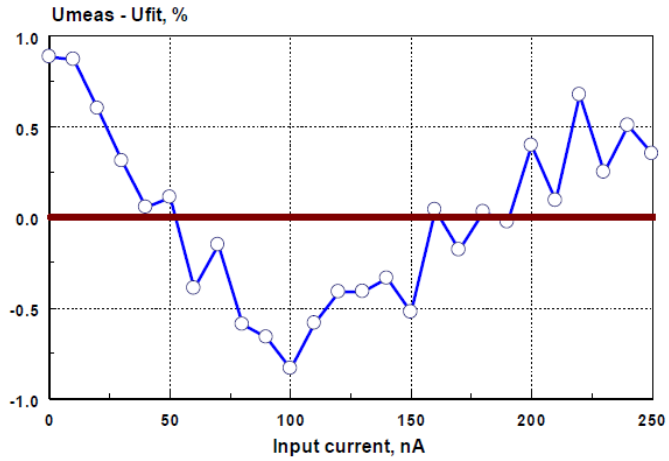
Sumačný zosilňovač

BB96 charakteristika





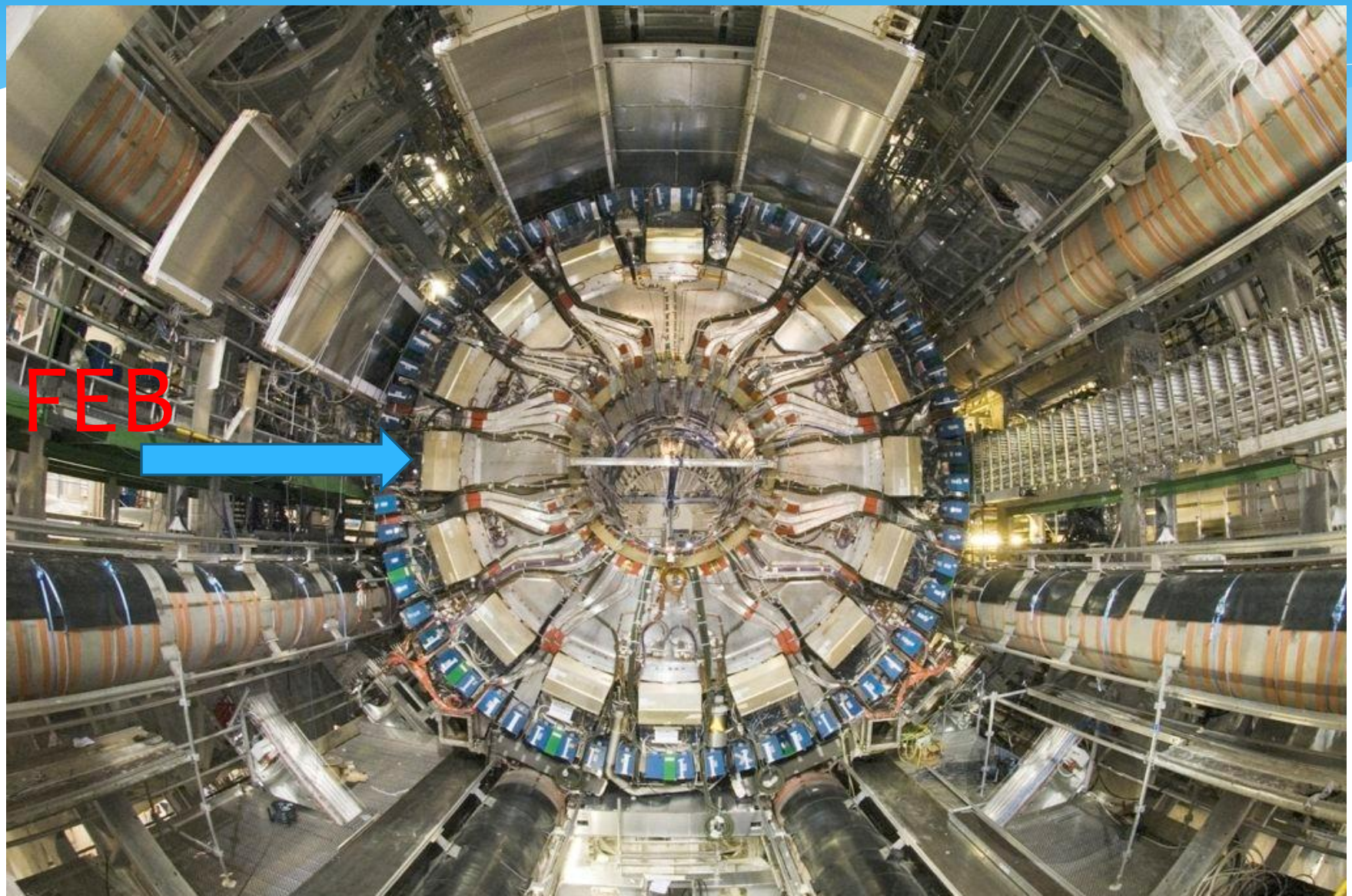




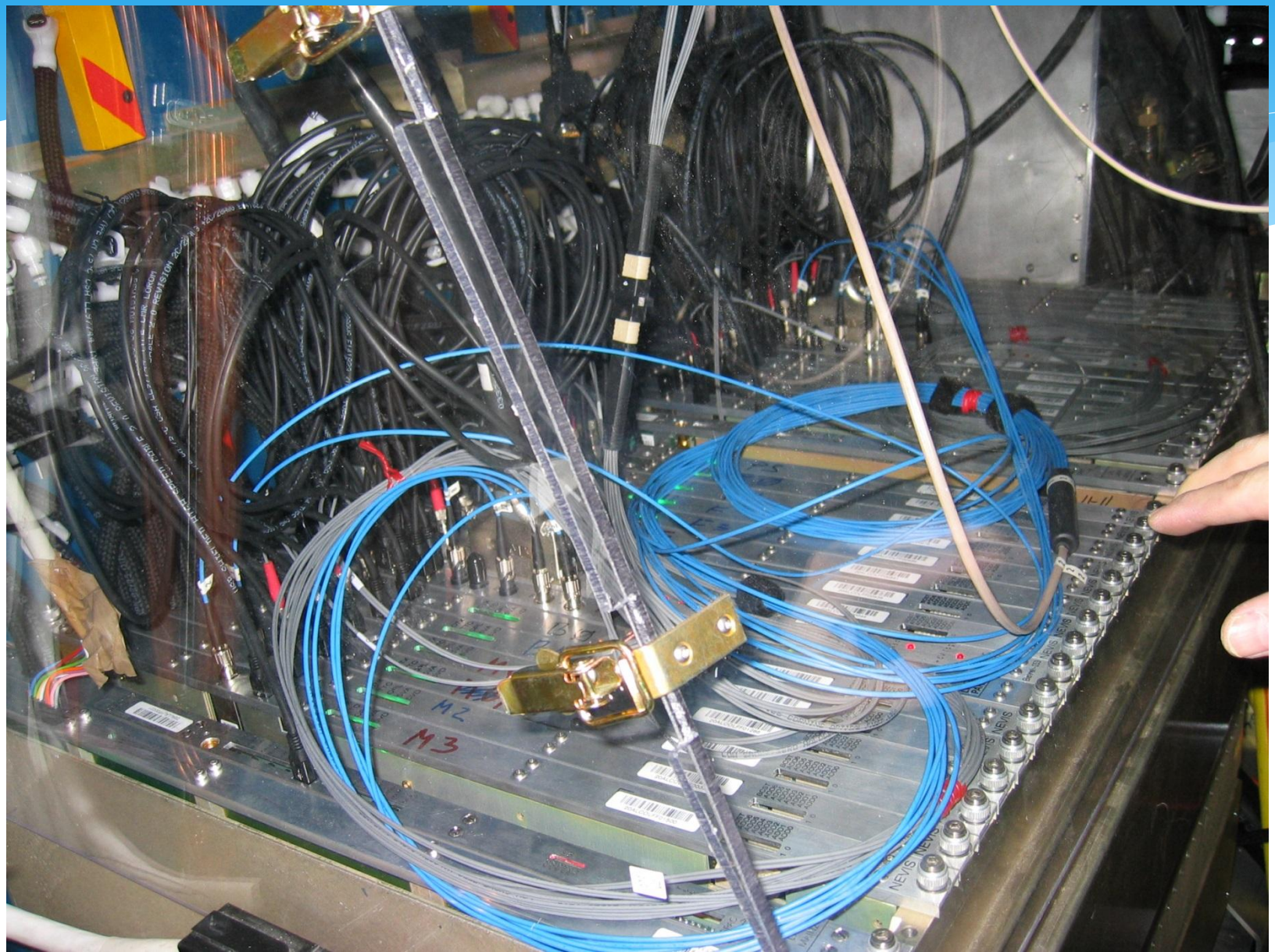
„Studená elektronika HEC“

* Elektronický obvod čípu BB96 bol navrhnutý tak aby fungoval v radiácii a veľkom rozsahu teplôt (-200 + 30 C)
* Studená elektronika (-200C) vyvinutá v roku 1996
* Inštalovaná v roku 2003-4 a doteraz predstavuje najväčší prevádzkovaný „studený “elektronický systém na svete
* Roky fungovania v Larg a radiácii povrdzujú dosiahnutie plánovaných parametrov a výkonnosti elektroniky

Front-end elektronika pre Larg



FE crate



Front-end board

Optický výstup

Časovanie celej dosky

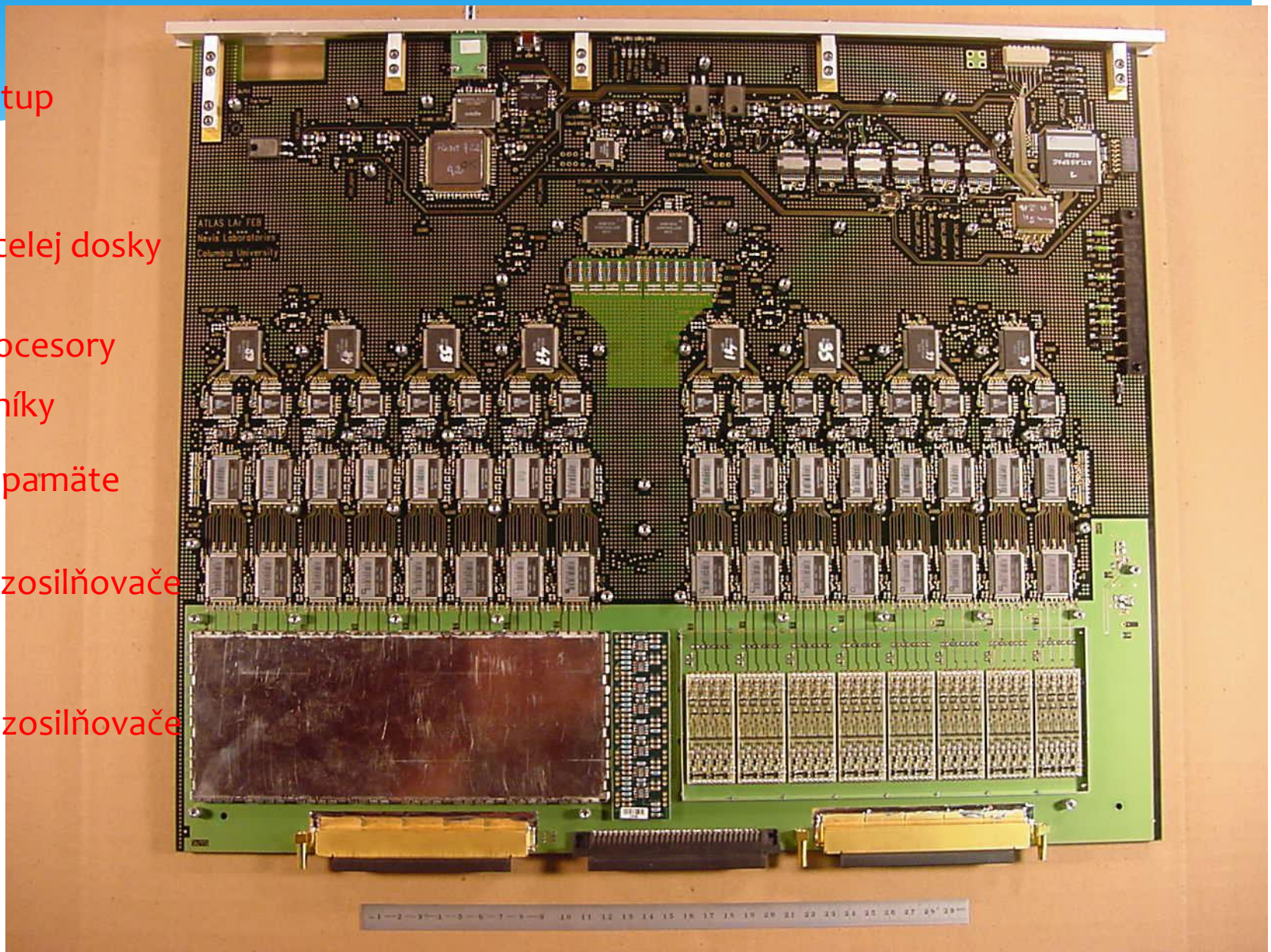
Digitálne pocesory

AD prevodníky

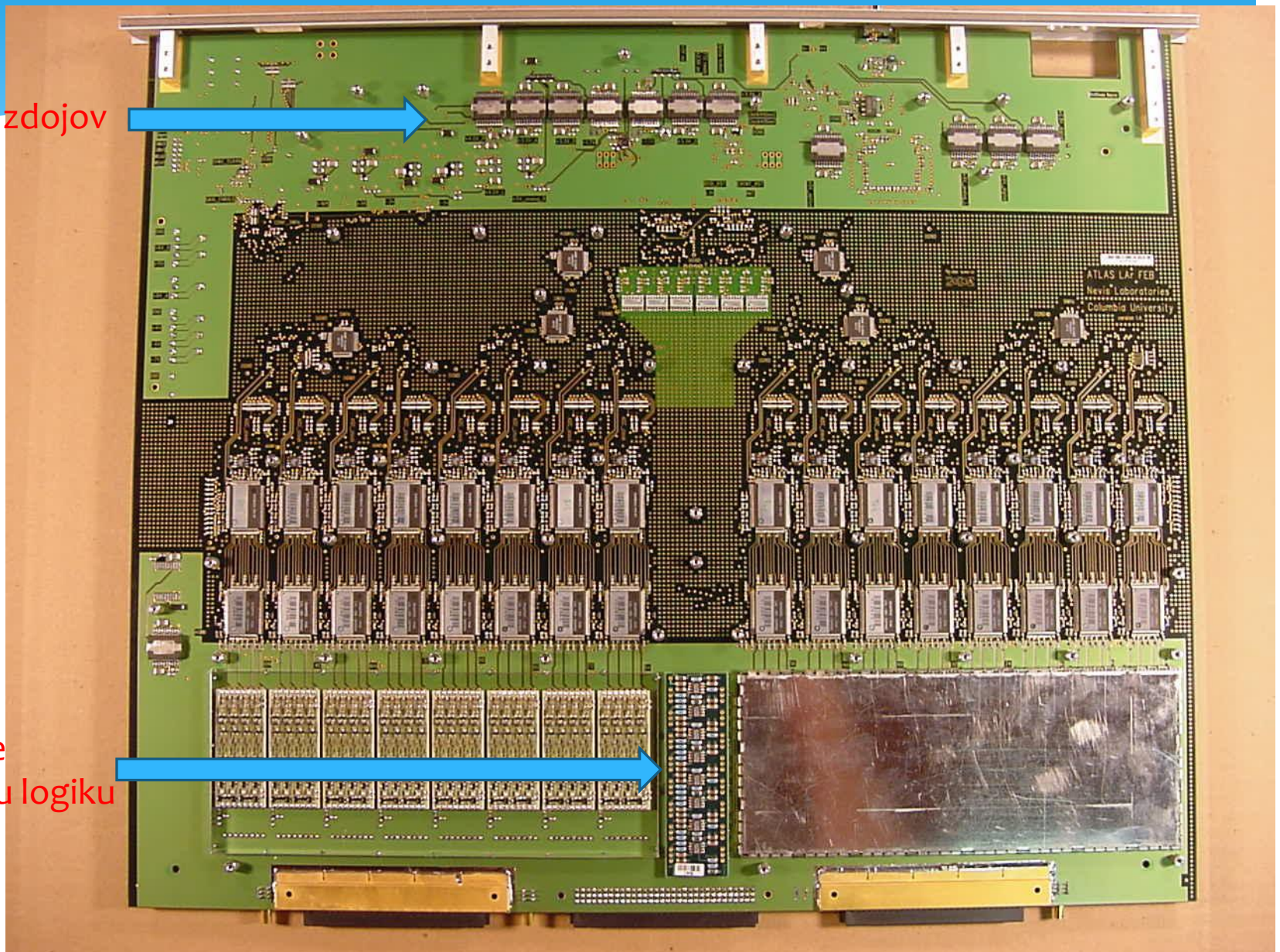
Analógové pamäte

Tvarovacie zosilňovače

Analogove zosilňovače



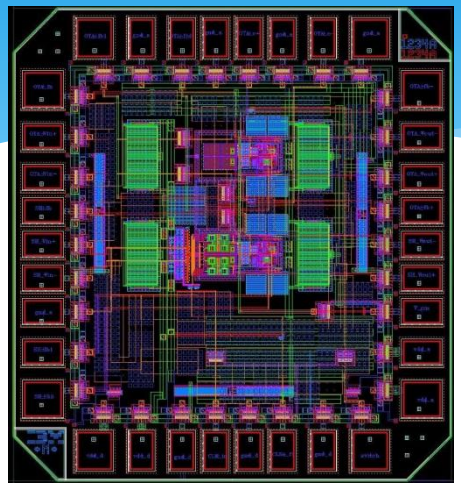
Front-end board

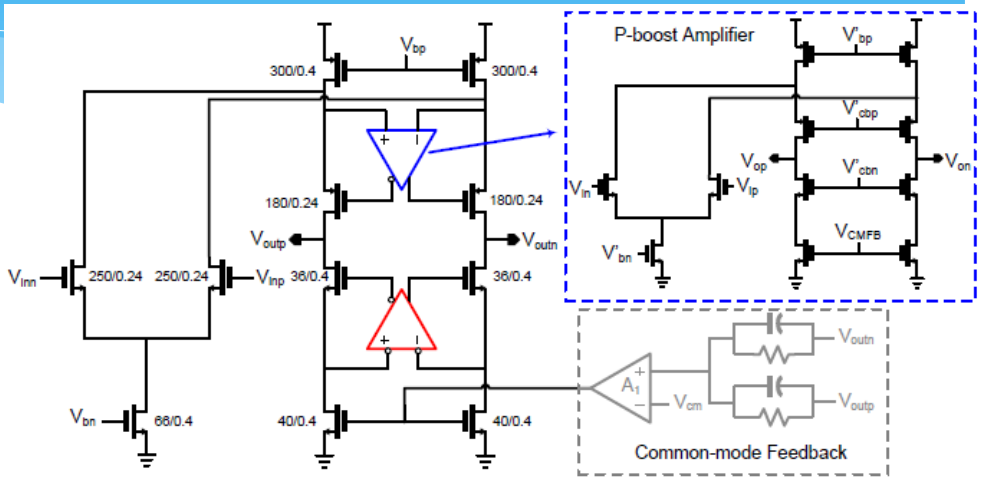


Front-end elektronika

* FEB doska predstavuje supercitlivú elektroniku s dynamickým rozsahom 16bit (merajúca prúdy v rozsahu nA - 10mA) a 12 bitovou presnosťou
* Vodou chladený (70W na dosku), radiačne odolný elektronický sytém skladajúci sa z 1560 dosiek
* Korelovaný šum celého systému je okolo 5% bieleho šumu
* Larg FEB systém je kľúčový pre experiment Atlas

Rad-hard ADC pre trigger and upgrade



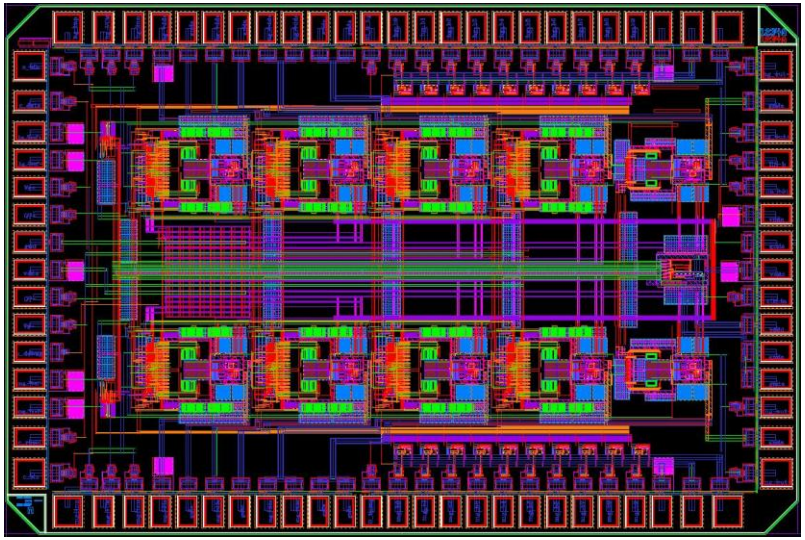


* Nevis09 chip
  - Operational trans-conductance amplifier (OTA) circuit developed
    * DC gain of > 80 dB, UGB of >450MHz, power ~8mW, VDD=2.5V
    * The design (schematics and layout) stayed unchanged in all the next chips
  - S/H circuit developed
  - Confirmed understanding of the technology (IBM CMOS 8RF 130nm)

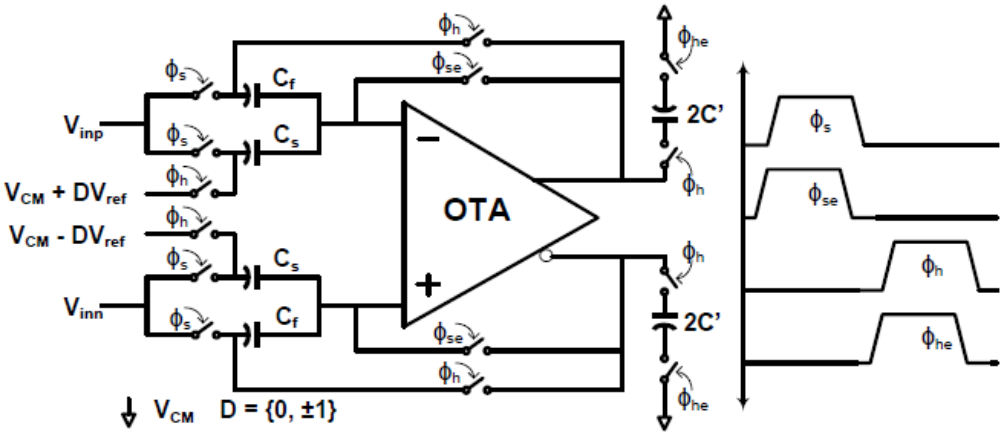
Rad-hard ADC pre trigger and upgrade

- Nevis10 chip
  - 2channels of 4MDACs working in pipeline mode
  - Gain selection structure implemented to test high resolution ADC using gain selection algorithms
    - R&D for phase-2
  - MDAC circuit with 12 bit performance developed
    - Flip-around architecture
    - Bottom plate sampling to 1pF capacitors
    - subADC with separate sampling
    - Flash comparator sized to comfortably meet subADC offset requirements
    - 1.5 bits/stage, i.e. 3 possible codes to resolve one bit → digital error correction to compensate for technology limitations (cap m
    - atching, gain,…)

Rad-hard ADC

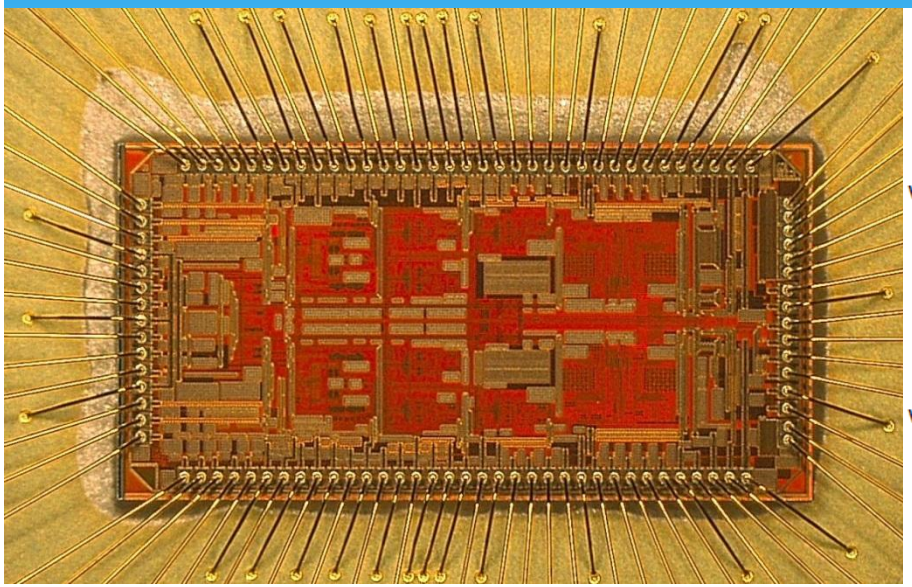


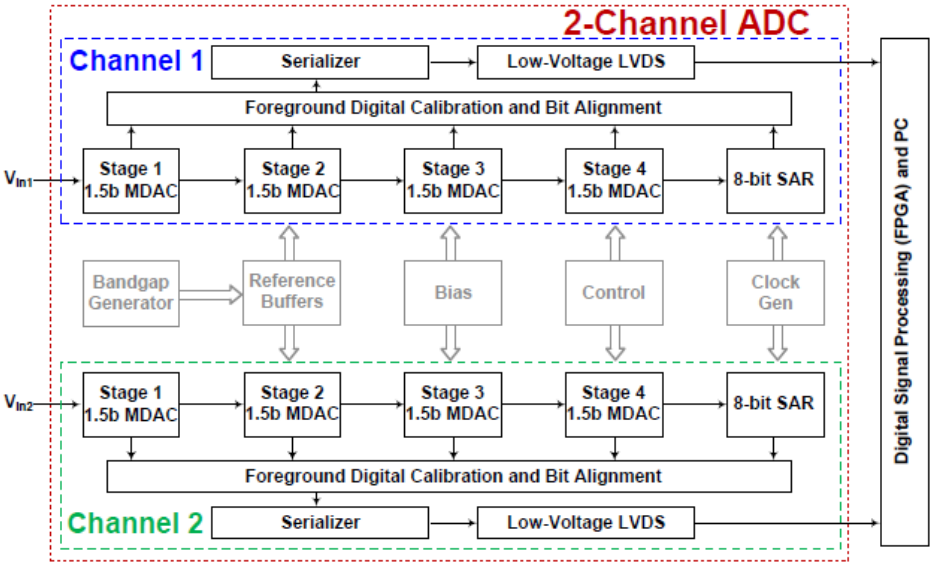
Nevis10 layout



MDAC block diagram (subADC not shown here)

Rad-hard ADC

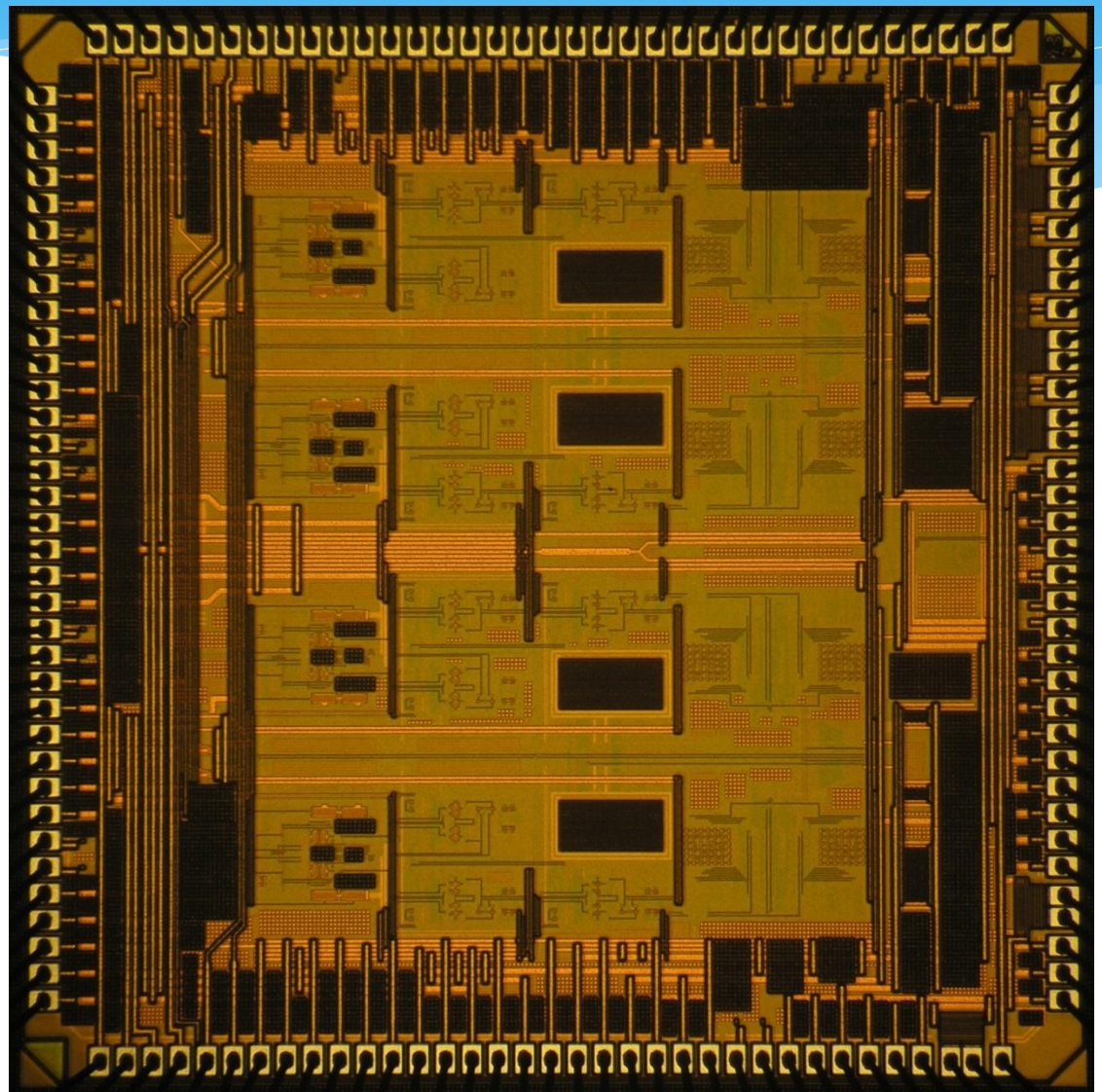




- Nevis12 chip : a big step toward the final design
  - 2 channels of 12 bit ADC
    - four (scaled down) 1.5b MDACs followed by 8 bit SAR unit
  - Two clock system (640MHz and 40MHz) with no PLL on the chip
  - Output data serializer unit
  - Foreground calibration constants computed outside the chip
  - Digital data processing unit
    - Triple redundant calibration constants stored/used on chip
    - Digital correction on the chip
  - 8 bit synchronous SAR unit
    - Synchronous operation at 640 MHz

Rad hard ADC (Nevis13)

* Final Layout
  * 3.6mmx3.6mm
  * 120 die pins
  * 48 GND down-bonds
  * 72pin QFN package



Rad-hard ADC

* Nevis13 chip features
  * 4 channels of 12bit ADC (4MDACs and 8bit SAR)
  * Sampling information derived from the rising edge of differential input SLVS 40MHz clock
  * Fast clock generated internally by PLL
  * Differential signal input of 2.4V FS with 1.25V common mode voltage
  * Reference voltages available on the I/O pins
  * Band-gap circuit designed at Cern
  * Power supply voltages: 1.2V and 2.5V
  * Conversion result available 87.5ns after sampling
  * Data sent out serially using 320MHz DDR SLVS clock signaling
  * Special “frame” signal marks MSB of shifted data
  * Calibration constants computed outside and applied inside the chip
  * I2C interface (1.2V signaling) allows to control all internal functions of the chip
  * Power dissipation of ~43mW/channel (preliminary measurement on few chips)

Rad hard ADC

* Vyvýjaný pre budúce experimentovanie na Atlase
* Nevis13-Nevis14 bude použitý v blízkej budúcnosti pre triggrovací systém Larg kalorimetra
* Úsilie slúži aj pre vývoj AD prevodníka pre budúcu generáciu FEB elektroniky

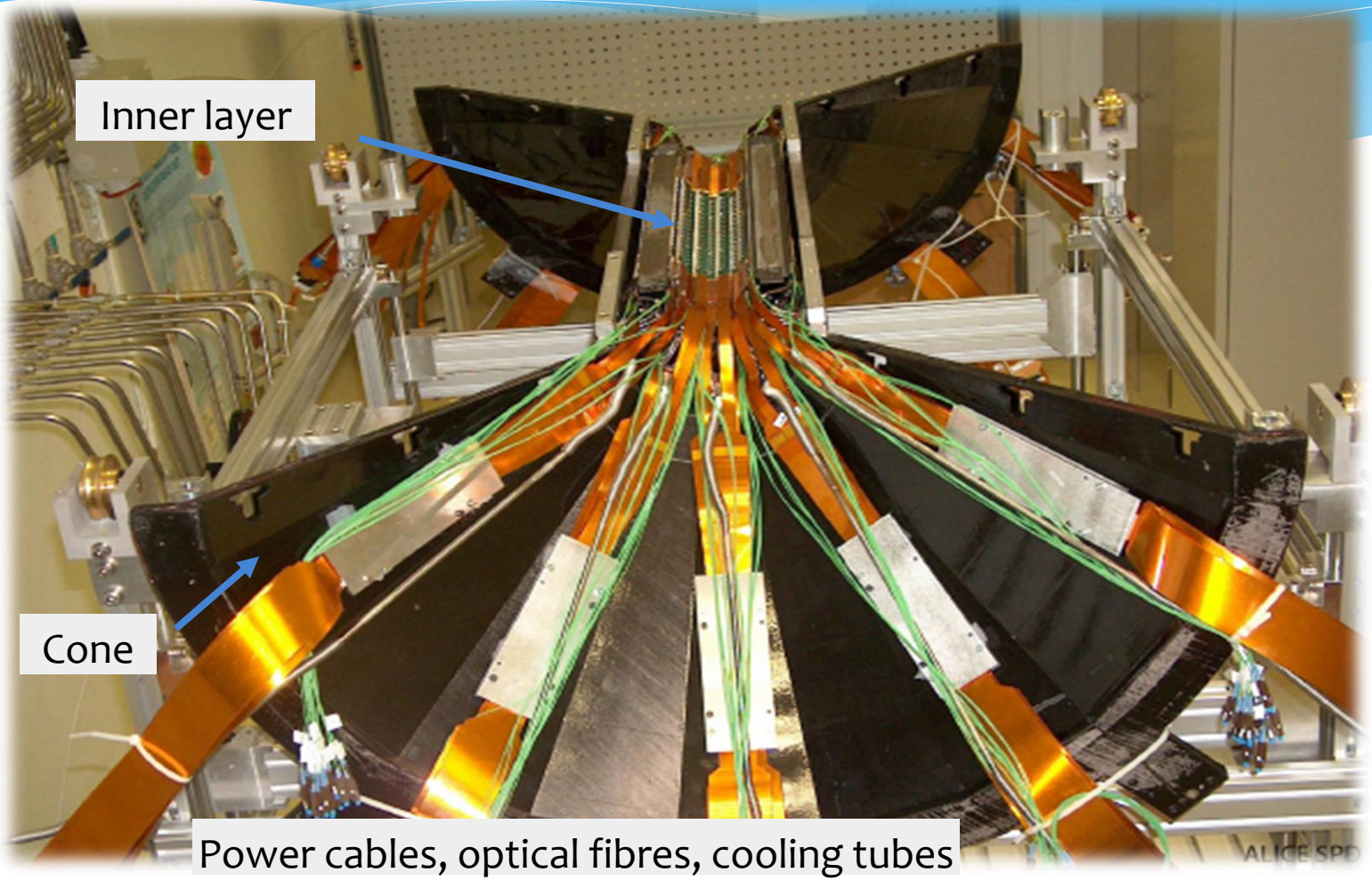
Elektronika pre experimenty ALICE a NA62

Predstavenie

* Ing. Marián Krivda, PhD. vedecký pracovník ÚEF SAV Košice a Research fellow na University of Birmingham, Birmingham, UK pracujúci na vývoji elektroniky pre experimenty ALICE a NA62.
* Hlavné oblasti vývoja elektroniky založenej na FPGA obvodoch:
  - Vyčítavacia a riadiacia elektronika pre kremíkový pixelový detektor (Silicon Pixel Detector -SPD) pre ALICE experiment
  - Triggrovacia elektronika pre experimenty ALICE a NA62
  - Front end elektronika pre CEDAR detektor pre NA62 experiment

http://mkrivda.web.cern.ch/mkrivda/work_page.htm

Silicon Pixel Detector (SPD) v experimente ALICE



SPD Router

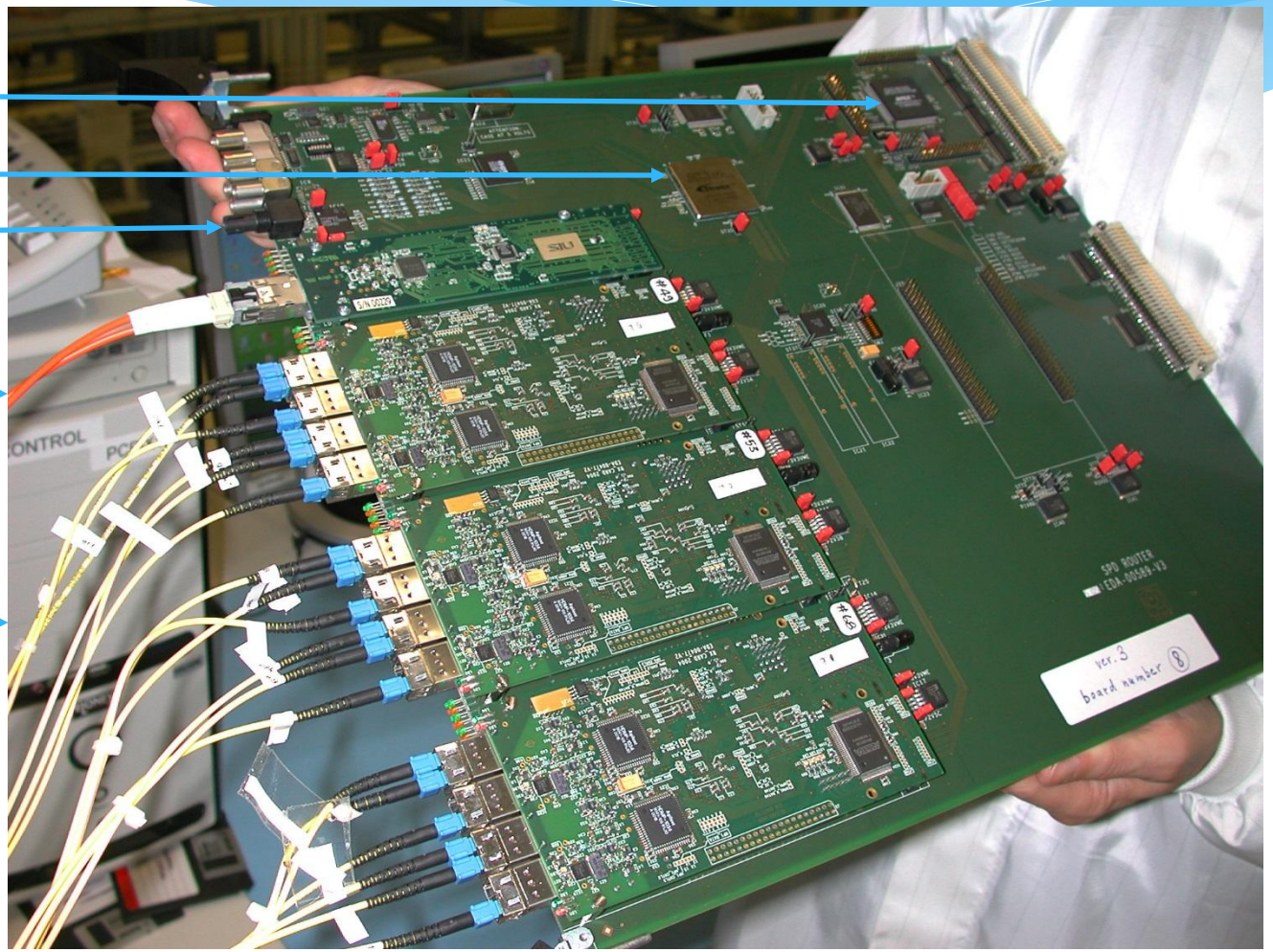
VME interface

FPGA Altera Stratix

Prijímač taktovacích hodín a triggrov

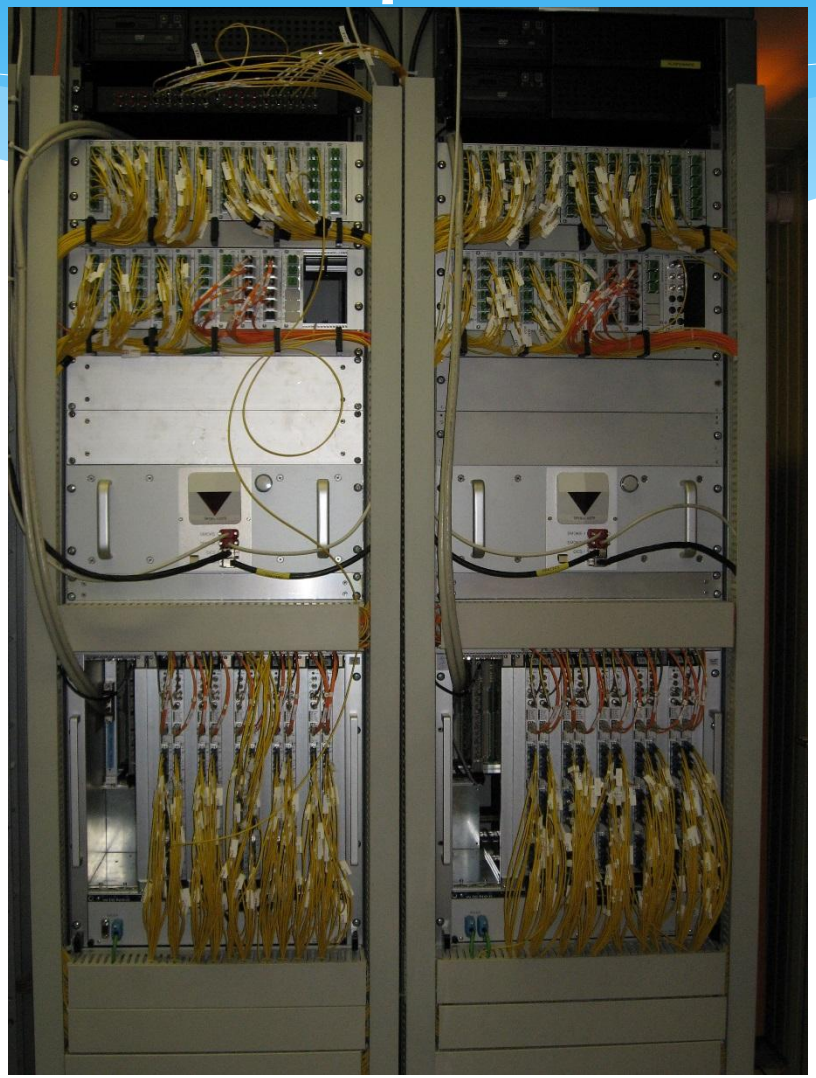
Optická linka do DAQ

Gigabitove optické linky z detektora



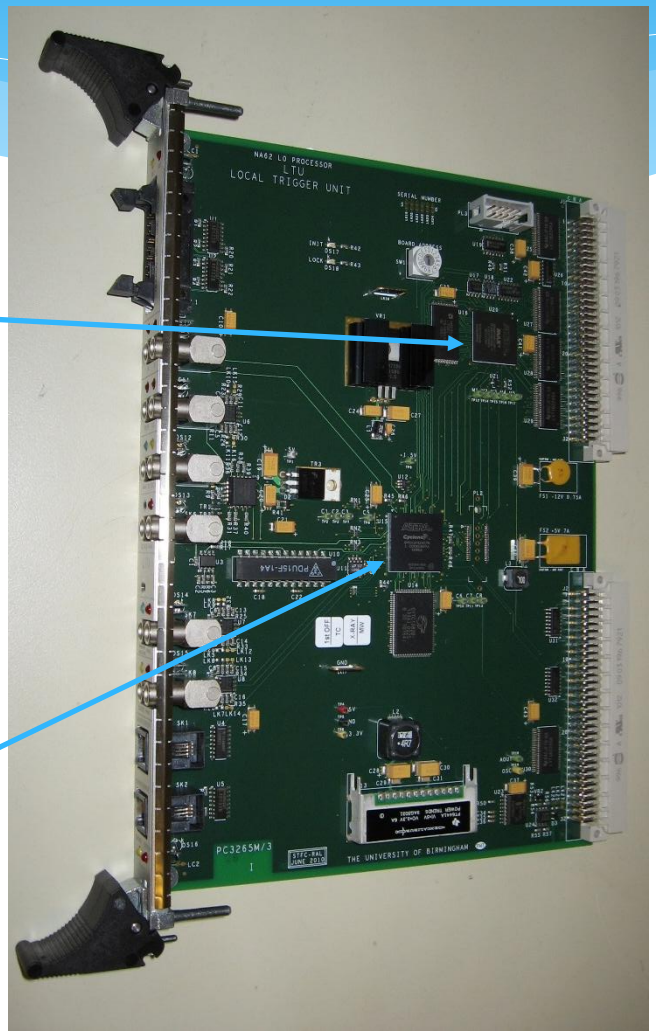
Kompletná elektronika pre SPD

* Vyčítanie dát z 10 mil. kanálov
* Formátovanie dát
* Redukcia dát na základe informácie z triggrovacieho systému
* Posielanie dát do centrálneho systému zberu dát (DAQ)



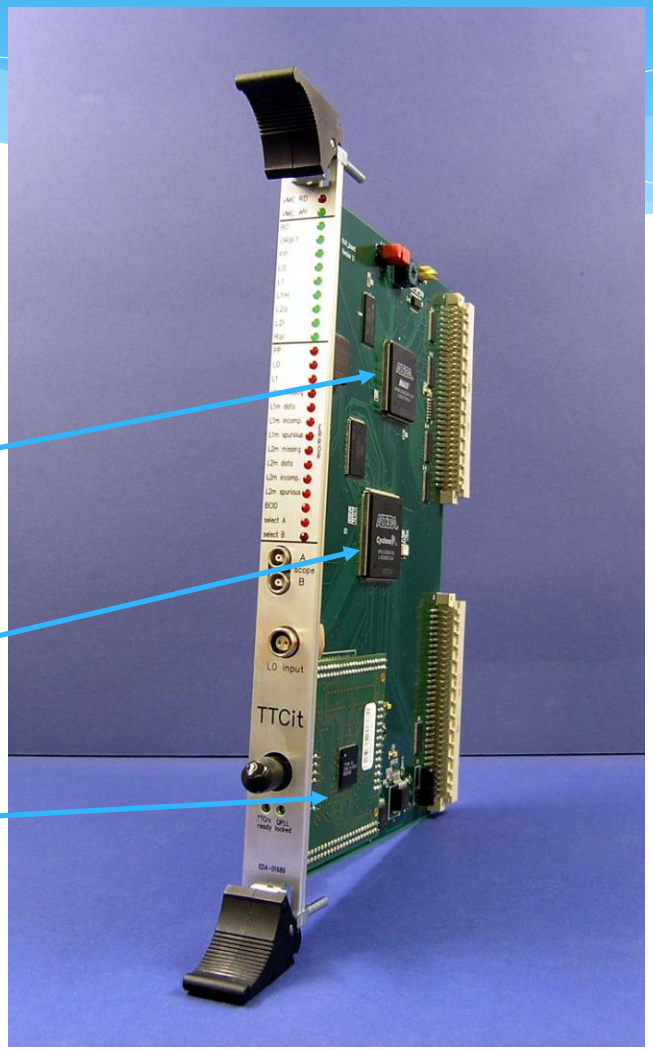
Local trigger unit

* Lokálny triggrovací modul pre experimenty ALICE a NA62
* Ovládanie cez VME rozhranie
* Slúži ako zdroj trigger signálov pre testovanie v laboratóriu alebo ako rozhranie medzi Centrálnym triggrovacím procesorom a detektorom
* Triggrovacia logika a formátovanie dát pre TTC systém je implementované v FPGA obvode ALTERA Cyclone



TTCit

* Monitorovanie TTC (Trigger and Timing Control) signálov pre experimenty ALICE a NA62
* Ovládanie cez VME rozhranie
* Monitorovacia logika je implementovaná v FPGA obvode ALTERA Cyclone
* TTCrq mezzanine doska ako prijímač TTC signálov



LMo triggrovací modul

USB-JTAG module

DC-DC konvertory

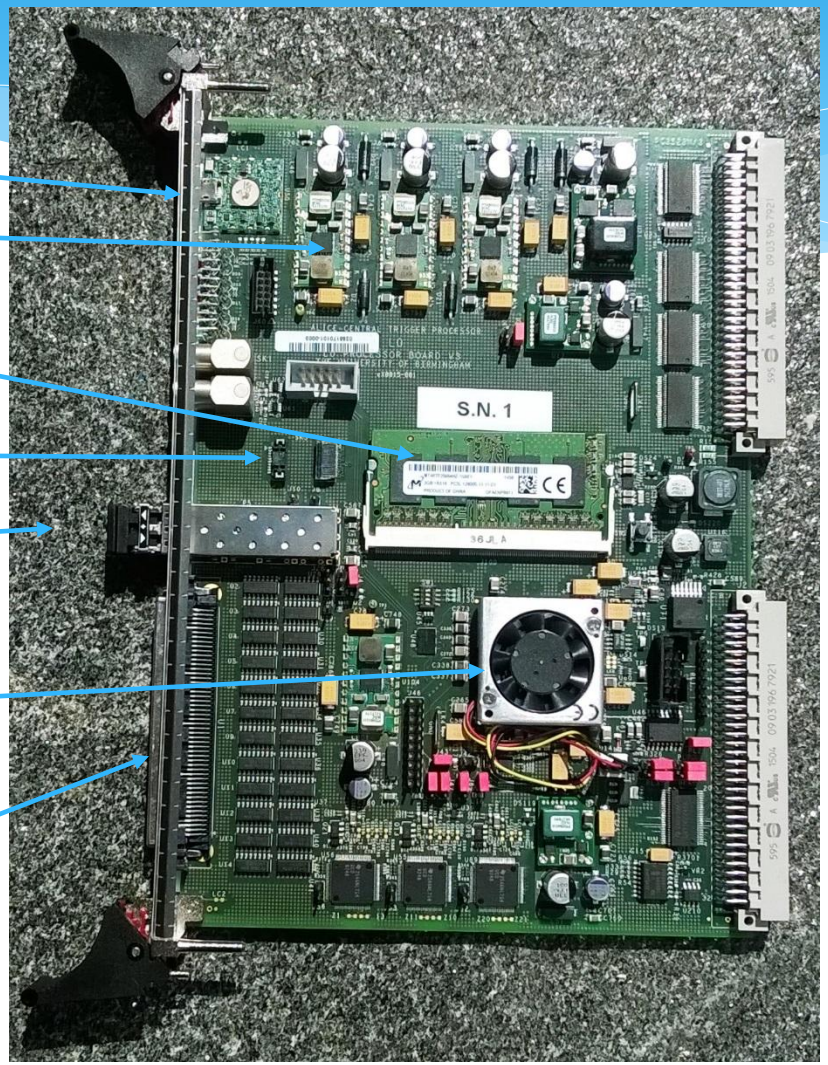
2 GB SODIMM

SAMTEC FireFly cable
(12 diff. links)

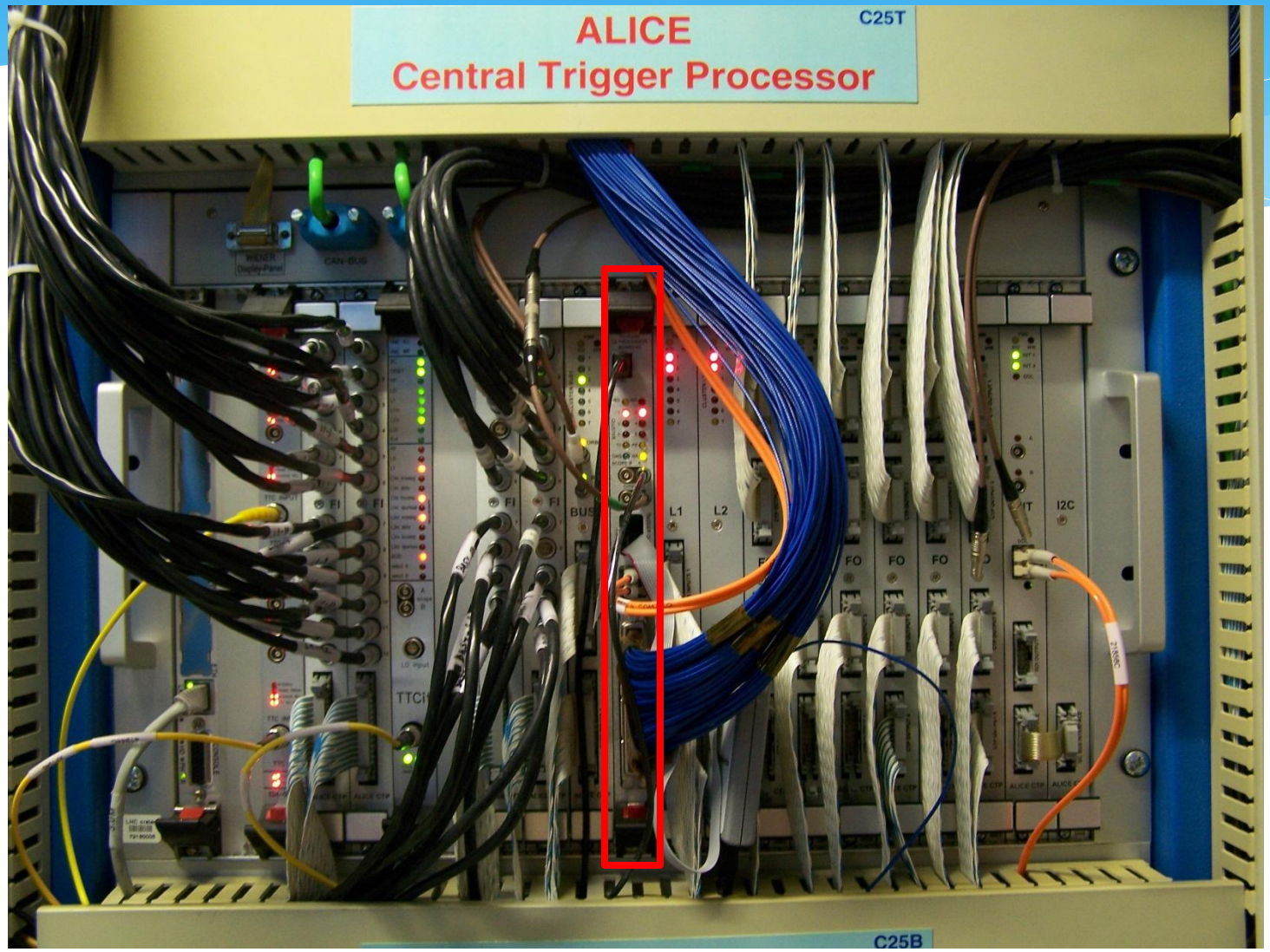
SFP+ link to DAQ

Xilinx Kintex-7 FPGA

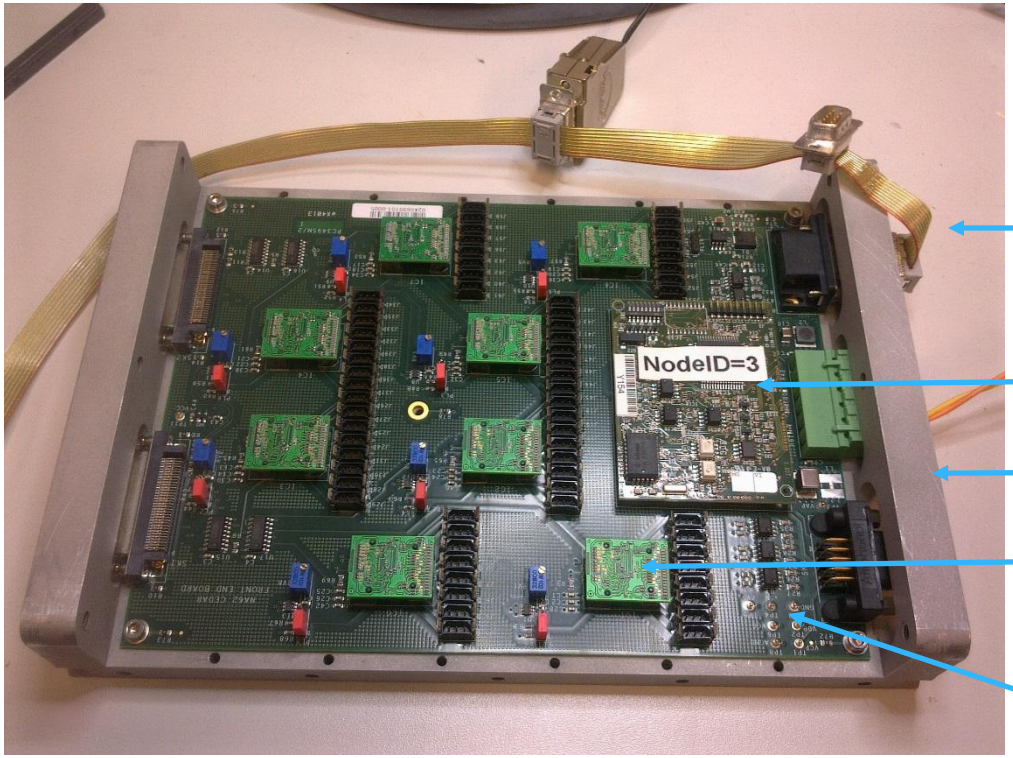
96 LVDS I/O
- Trigger inputs
- BUSY inputs
- LM output



LMo modul nainštalovaný v CTP



Front end elektronika pre CEDAR detektor pre NA62 experiment



CAN bus rozhranie

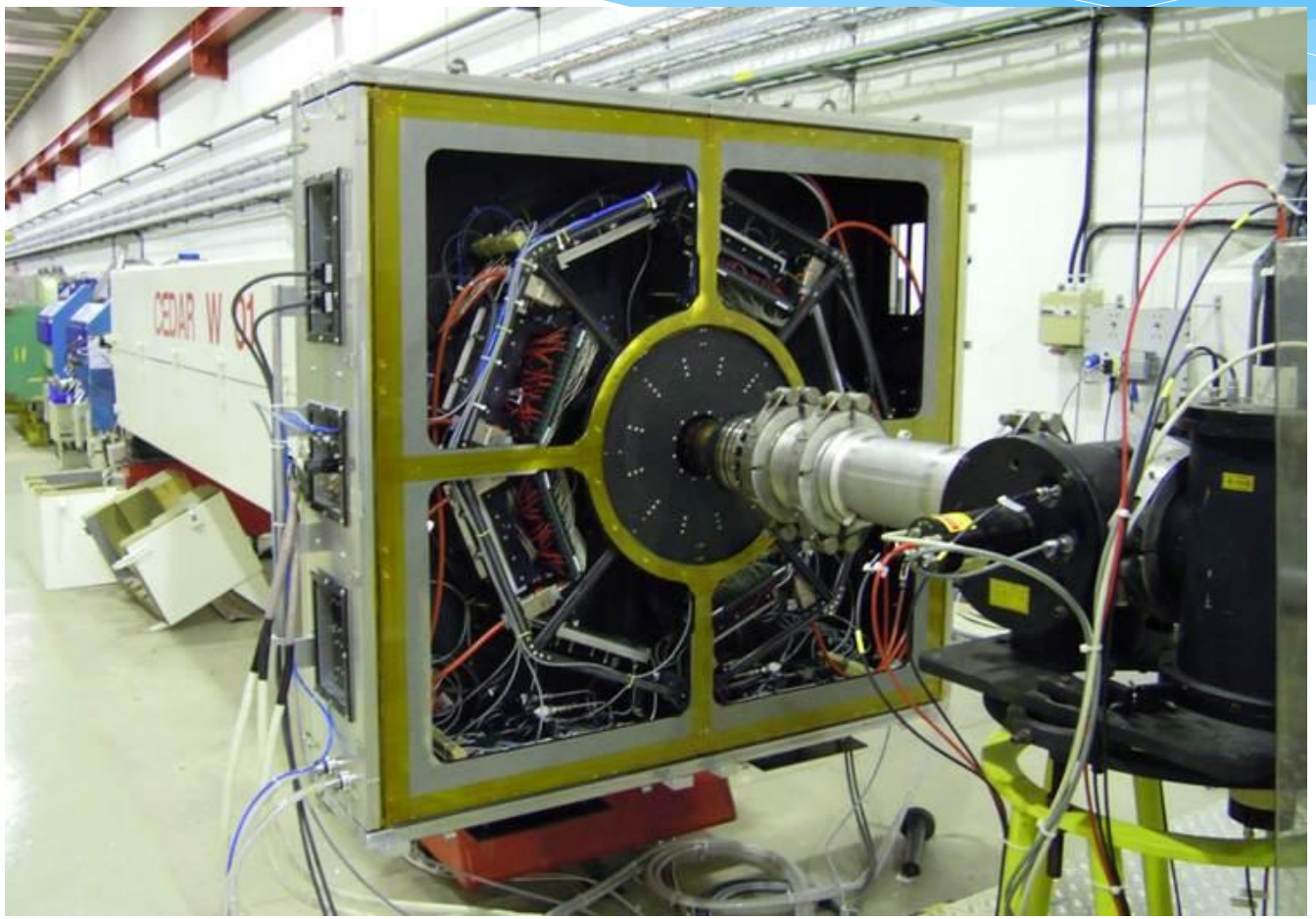
ELMB controller

chladič

NINO čipy na mezzanine doštičke

Napäťový regulátor (zo spodnej strany PCB)

Nainštalovaná front end elektronika pre CEDAR detektor pre Na62 experiment



Záver

* Cern represents a hope for Slovak young people to become „best of the best“ engineers
* Take the chance before you and make your life challenging, hard and sometimes difficult
* This is the one of few things you will be proud of at the end of your life